A MONOLITHIC GaAs 0.1 TO 10 GHz AMPLIFIER*

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ABSTRACT

A monolithic GaAs 4-stage broadband amplifier including active input and output matching has been fabricated on a 2.5 mm square chip. Gain, noise, and VSWR performance in the 0.1 to 10 GHz band will be described.

A monolithic GaAs low noise amplifier for operation from 0.1 to 10 GHz has been designed and fabricated using ion implantation technology. The 4-stage circuit consists of an active input matching network, two gain stages, and an active output matching network on a compact 2.5 mm square chip. Gain levelling, bias circuitry, and RF bypassing are included on chip for accurate characterization and ease of use. Gain and noise performance as well as input and output VSWR measurements will be presented following a description of the circuit design.

The circuit design requires use of both low and high frequency techniques due to the wide bandwidth of the amplifier. Low frequency gain is achieved in a small chip area by resistive loading of the FETs and minimum use of blocking capacitors. High frequency gain is achieved by reactive matching which is used in conjunction with resistive loads for improved gain slope compensation. Active matching, consisting of a common gate input stage and a source follower output stage, provides excellent VSWR performance while maintaining noise performance across the band. Figure 1 is a schematic of the broadband amplifier excluding parasitic elements. A 300 ohm resistor provides a low noise self-bias for the 300 micron wide common gate stage which in turn provides excellent input VSWR over most of the band. The inductive input transmission line helps tune the gate capacitance near the high end of the band and extends the input match to well above 10 GHz. The drain is inductively tuned to the common source second stage and is loaded by an 800 ohm resistor for low frequency gain control. A small source inductance in the second stage moves the gain and noise match closer together. An inductively isolated 22 ohm resistor on the drain provides substantial low end gain compensation and aids the high frequency peaking of the amplifier. Following a 10 pF blocking capacitor, at a high impedance point in the circuit, the resistively loaded common source third stage provides additional gain. Finally, a resistively self-biased common drain (or source follower) stage provides an impedance transformation and an excellent output match over the entire band. All bias bonding pad bypass capacitors are included on the chip to reduce gain variations due to variations in bond wire lengths. Of particular note is the 50 pF bypass capacitor for the 22 ohm gain compensation resistor.

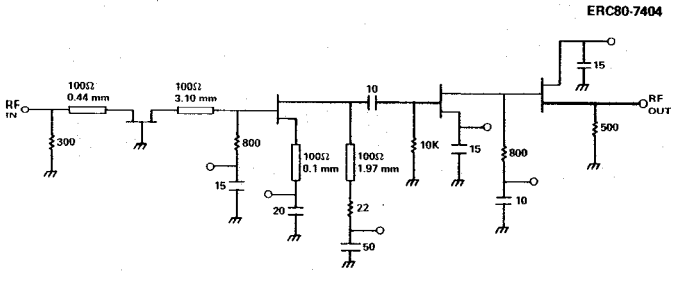

FIGURE 1: BROADBAND AMPLIFIER SCHEMATIC.

Calculated amplifier performance based on the initial design data is shown in Figure 2. The computer model used in the gain and noise figure predictions includes lossy distributed elements with dispersion and parasitic coupling capacitances between adjacent circuit elements. Separate FET parameters are used for each stage to reflect the various bias points. As shown in Figure 1, noise figure is predicted to be 4 dB; however, transmission line losses are not included in the noise figure calcualtions. Although not shown, the input and output VSWR into 50 ohms are calculated to be better than 1.25:1 over the entire band.

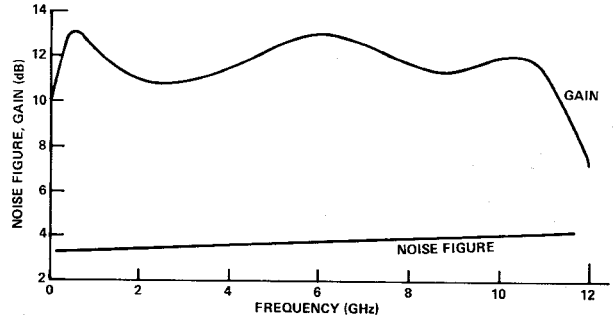

FIGURE 2: PREDICTED BROADBAND AMPLIFIER PERFORMANCE

The design is implemented as a microstrip circuit on a semi-insulating GaAs substrate containing lumped and distributed elements, ion implanted resistors, MIM capacitors, and FETs. Both Cr doped and undoped S.I. substrates grown by the horizontal Bridgman and the liquid encapsulated Czochralski (LEC) techniques have been used for device fabrication. A preselection test for bulk S.I. GaAs substrates involving qualification of the entire GaAs ingot by sampling the front and the tail of each boule is first employed to select the ingot to be used. The qualification procedure assesses the ability of the S.I. substrate to withstand high temperature (850°C) processing and to yield device quality active layers by ion implantation. Direct implantation of Si^+ in selected areas, defined photolithographically, is used for forming the FET and resistor active areas. The wafer is then coated with reactively sputtered Si_3N_4 and annealed at 850°C in an H_2 ambient resulting in active layers of ~1000 Ω/□ sheet resistivity and 4000-4500 cm/2 V-sec Hall mobility at 1×10^{17} cm^{-3} doping concentration. The use of ion implanted resistors implies that the final resistance will scale inversely with the I_{DSS} of the FETs ensuring proper biasing for a fairly large range of

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pinch off voltages. AuGe/Ni is used to form the ohmic contacts. The 1 μm long gates and the first level metallization are defined by conventional photolithography and liftoff process.[1] Gate metal is Ti/Pt/Au for good reliability. A dielectric layer of Si_3N_4 is used for the insulation between the first level and the second level interconnections and dielectric for the circuit MIM capacitors. Typically, 130 pF/mm² capacitance is obtained. Capacitance uniformity and reproducibility can generally be maintained to within ±5%. Reactive ion etching is used to open via holes in the dielectric wherever the first level metallization needs to be assessed. Second level metallization is formed by gold plated to a thickness of 2-3 μm to reduce RF losses in the passive circuitry. The GaAs wafer is thinned to 250 μm and metallized on the back to complete the ground plane of the microstrip transmission lines. The RF circuitry which controls the tuning is predominantly defined on the thick second level metallization. This provides the capability of modifying the tuning elements by altering only one mask level. Since this mask does not contain stringent dimensional tolerances, it is relatively simple to incorporate and evaluate design modifications as required. Only changes in resistor values, FETs and, major changes in capacitance values require the alteration of other mask levels. Figure 3 is an SEM photograph of the 2.5 mm square chip. The choice of a 10 mil substrate thickness is a compromise between the need for a thick substrate to obtain low-loss high-impedance transmission lines and the need for a thin substrate to achieve low interelement coupling and small chip size. Since power dissipation is low, the thermal resistance of the GaAs substrate is not a major consideration.

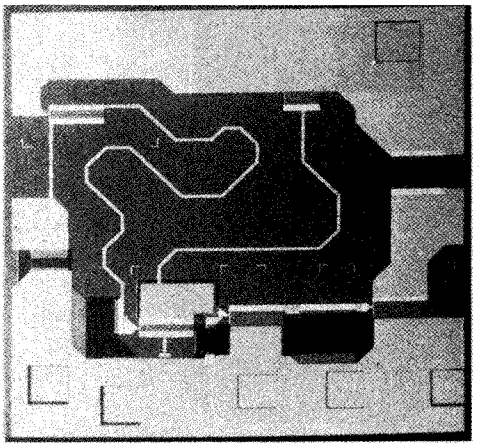

FIGURE 3: SEM PHOTOGRAPH OF THE MONOLITHIC AMPLIFIER CHIP

Figure 4 is a plot of the amplifier gain measured in a microstrip test fixture. As shown, the gain is 7.7 dB ± 0.8 dB from 2 to 8 GHz, 7 dB ± 1 dB from 700 MHz to 9 GHz. Further improvements in gain and gain flatness are expected with minor circuit modifications derived from more accurate computer models of the active and passive chip components. Measured input and output match are shown in Figure 5. Input and output VSWR are better than 2:1 from 100 MHz to over 12 GHz and better than 1.5:1 over most of the band. A spot noise figure measurement at 8 GHz yielded a noise figure of 6.8 dB.

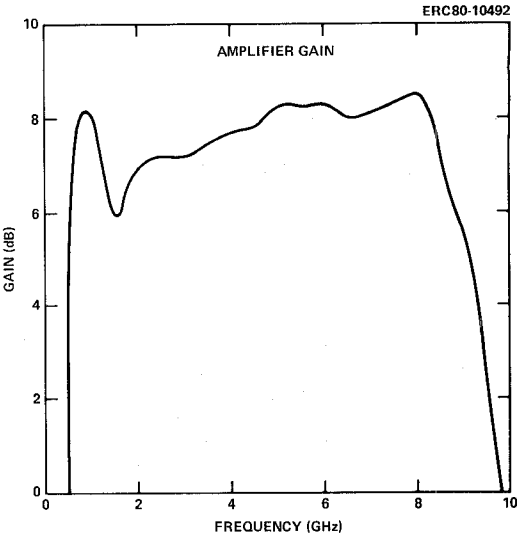

FIGURE 4: AMPLIFIER GAIN

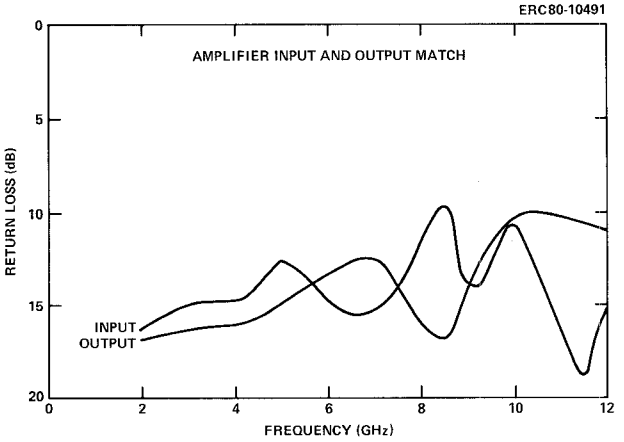

FIGURE 5: AMPLIFIER INPUT AND OUTPUT MATCH

References

1. A. K. Gupta, W. Petersen, "Monolithic GaAs Superheterodyne Front End," Interim Report No. 251-035/6-2-78, 427, Office of Naval Research, May 1980.